Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A data transfer control device for transferring data among a plurality of nodes that are connected to a bus, the data transfer control device comprising:

a transfer execution circuit that operates when a processing ~~means~~ section has issued a first start command which instructs continuous packet transfer by hardware, for executing processing to divide transfer data into a series of packets and transfer the thus divided series of packets continuously; and

an arbitration circuit that operates when the processing ~~means~~ section as issued a second start command which instructs packet transfer while continuous packet transfer processing is being executed by the transfer execution circuit, for waiting until one transaction or one packet transfer in the continuous packet transfer has been completed then permitting packet transfer by the second start ~~command~~ command, the processing section permitting the packet transfer by the second start command regardless of characteristics of the first start command and characteristics of the second start command.

2. (Currently Amended) ~~The data transfer control device as defined in claim 1,~~ ~~wherein~~ A data transfer control device for transferring data among a plurality of nodes that are connected to a bus, the data transfer control device comprising:

a transfer execution circuit that operates when a processing section has issued a first start command which instructs continuous packet transfer by hardware, for executing processing to divide transfer data into a series of packets and transfer the thus divided series of packets continuously; and

an arbitration circuit that operates when the processing section has issued a second start command which instructs packet transfer while continuous packet transfer processing is being executed by the transfer execution circuit, for waiting until one transaction or one packet transfer in the continuous packet transfer has been completed then permitting packet transfer by the second start command,

the transfer execution circuit ~~comprises~~ including at least one of:

a page table fetch circuit that operates when a page table exists in a storage ~~means~~ memory of another node, to fetch the page table from the other node;

a page table creation circuit that operates when no page table exists in the storage ~~means~~ memory of the other node, to create a virtual page table, based on page boundary information;

a payload division circuit for dividing transfer data into packets of a payload size;

a transfer execution control circuit for controlling the execution of data transfer; and

a control information creation circuit for creating control information of a request packet to be sent to the other node.

3. (Currently Amended) The data transfer control device as defined in claim 1, ~~wherein~~ the arbitration circuit ~~receives~~ receiving a first start signal that goes active when there is a transfer start request from the transfer execution circuit, a second start signal that goes active when there is a transfer start request in accordance with the second start command, and a completion signal that goes active at transfer completion; then ~~causes~~ causing the start of transfer processing in accordance with the first start signal when the second start signal went active after the first start signal had gone active, and ~~causes~~ causing

the start of transfer processing in accordance with the second start signal after the completion signal goes active.

4. (Currently Amended) The data transfer control device as defined in claim 1, ~~wherein~~ the arbitration circuit ~~receives~~ receiving a first start signal that goes active when there is a transfer start request from the transfer execution circuit, a second start signal that goes active when there is a transfer start request in accordance with the second start command, and a completion signal that goes active at transfer completion; and ~~gives~~ giving priority to transfer processing in accordance with the second start signal when the first and second start signals have gone active together.

5. (Currently Amended) The data transfer control device as defined in claim 1, ~~wherein~~ the arbitration circuit ~~receives~~ receiving a first start signal that goes active when there is a transfer start request from the transfer execution circuit, a second start signal that goes active when there is a transfer start request in accordance with the second start command, and a completion signal that goes active at transfer completion; then ~~causes~~ causing the start of transfer processing in accordance with the second start signal when the first start signal went active after the second start signal had gone active, and ~~causes~~ causing the start of transfer processing in accordance with the first start signal after the completion signal goes active.

6. (Currently Amended) ~~The data transfer control device as defined in claim 1, further comprising:~~ A data transfer control device for transferring data among a plurality of nodes that are connected to a bus, the data transfer control device comprising:

a transfer execution circuit that operates when a processing section has issued a first start command which instructs continuous packet transfer by hardware, for executing processing to divide transfer data into a series of packets and transfer the thus divided series of packets continuously; and

an arbitration circuit that operates when the processing section has issued a second start command which instructs packet transfer while continuous packet transfer processing is being executed by the transfer execution circuit, for waiting until one transaction or one packet transfer in the continuous packet transfer has been completed then permitting packet transfer by the second start command;

randomly accessible packet storage ~~means~~ memory having a control information area for storing packet control information and a data area for storing packet data; and

an address generation circuit ~~for generating~~ which generates a write address to the packet storage ~~means~~ memory,

~~wherein~~ the control information area of the packet storage means ~~is~~ memory being separated into a first control information area and a second control information area, control information of the second control information area being written by the transfer execution ~~circuit; and~~ circuit, and

~~wherein~~ the address generation circuit ~~switches~~ switching between generating addresses for the first control information area and addresses for the second control information area, based on an arbitration result from the arbitration circuit.

7. (Currently Amended) ~~The data transfer control device as defined in claim 1, further comprising:~~ A data transfer control device for transferring data among a plurality of nodes that are connected to a bus, the data transfer control device comprising:

a transfer execution circuit that operates when a processing section has issued a first start command which instructs continuous packet transfer by hardware, for executing processing to divide transfer data into a series of packets and transfer the thus divided series of packets continuously; and

an arbitration circuit that operates when the processing section has issued a second start command which instructs packet transfer while continuous packet transfer processing is being executed by the transfer execution circuit, for waiting until one transaction or one packet transfer in the continuous packet transfer has been completed then permitting packet transfer by the second start command; and

randomly accessible packet storage ~~means~~ memory having a control information area for storing packet control information and a data area for storing packet data,

~~wherein~~ the data area of the packet storage means ~~is~~ memory being separated into a first data area for storing first data for a first layer and a second data area for storing second data for a second layer that is the object of continuous packet transfer by the transfer execution circuit.

8. (Currently Amended) The data transfer control device as defined in claim 7,

~~wherein,~~ when a request packet for starting a transaction is transmitted to another node, instruction information for instructing the processing to be performed when a response packet will be received from the other node ~~is comprised~~ being included within transaction identification information in the request packet; and

~~wherein,~~ when a response packet is received from the other node, control information and first and second data of the response packet ~~are~~ being respectively written to the control information area and the first and second data areas, based on the instruction information comprised within the transaction identification information in the response packet.

9. (Currently Amended) The data transfer control device as defined in claim 1,

~~wherein~~ data transfer is performed in accordance with the IEEE 1394 standard.

10. (Original) Electronic equipment comprising:

the data transfer control device as defined in claim 1;

a device for performing given processing on data that has been received from another node via the data transfer control device and the bus; and

a device for outputting or storing data that has been subjected to the processing.

11. (Original) Electronic equipment comprising:

the data transfer control device as defined in claim 2;

a device for performing given processing on data that has been received from another node via the data transfer control device and the bus; and

a device for outputting or storing data that has been subjected to the processing.

12. (Original) Electronic equipment comprising:

the data transfer control device as defined in claim 6;

a device for performing given processing on data that has been received from another node via the data transfer control device and the bus; and

a device for outputting or storing data that has been subjected to the processing.

13. (Original) Electronic equipment comprising:

the data transfer control device as defined in claim 7;

a device for performing given processing on data that has been received from another node via the data transfer control device and the bus; and

a device for outputting or storing data that has been subjected to the processing.

14. (Original) Electronic equipment comprising:

the data transfer control device as defined in claim 9;

a device for performing given processing on data that has been received from another node via the data transfer control device and the bus; and

a device for outputting or storing data that has been subjected to the processing.

15. (Original) Electronic equipment comprising:

the data transfer control device as defined in claim 1;

a device for performing given processing on data that is to be transferred to another node via the data transfer control device and the bus; and

a device for fetching data to be subjected to the processing.

16. (Original) Electronic equipment comprising:

the data transfer control device as defined in claim 2;

a device for performing given processing on data that is to be transferred to another node via the data transfer control device and the bus; and

a device for fetching data to be subjected to the processing.

17. (Original) Electronic equipment comprising:

the data transfer control device as defined in claim 6;

a device for performing given processing on data that is to be transferred to another node via the data transfer control

device and the bus; and

a device for fetching data to be subjected to the processing.

18. (Original) Electronic equipment comprising:

the data transfer control device as defined in claim 7;

a device for performing given processing on data that is to be transferred to another node via the data transfer control device and the bus; and

a device for fetching data to be subjected to the processing.

19. (Original) Electronic equipment comprising:

the data transfer control device as defined in claim 9;

a device for performing given processing on data that is to be transferred to another node via the data transfer control device and the bus; and

a device for fetching data to be subjected to the processing.

20. (New) The data transfer control device as defined in claim 2, data transfer is performed in accordance with the IEEE 1394 standard.

21. (New) The data transfer control device as defined in claim 6, data transfer is performed in accordance with the IEEE 1394 standard.

22. (New) The data transfer control device as defined in claim 7, data transfer is performed in accordance with the IEEE 1394 standard.